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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/064,214	06/21/2002	Ching-Hsiang Hsu	EMEP0011USA	2835

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EXAMINER

HO, HOAI V

ART UNIT

PAPER NUMBER

2818

DATE MAILED: 07/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/064,214

Applicant(s)

HSU ET AL.

Examiner

Hoai V. Ho

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1 and 5-9 is/are rejected.
- 7) ☒ Claim(s) 2-4 and 10 is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 21 June 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on ____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) ____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

1. Claims 1-10 are presented for examination.

Specification

2. The disclosure is objected to because of the following informalities:

A "bit line voltage (V_{BL}) is applied to the P^+ doped source region 134 of the first PMOS transistor 101" in a paragraph [0026] of a specification is contrary to "the P^+ doped drain region 132 of the first PMOS transistor 101 is electrically connected with a bit line 170 through contact plug 20" in a paragraph [0024] (see fig. 3A). Does the bit line voltage (V_{BL}) apply to the P^+ doped drain region 132 of the first PMOS transistor 101 instead as shown in figures 3A and 3B?

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible errors as above. Applicants' cooperation is requested in correcting any errors of which applicant may become aware in the specification if the above objection of the specification is correct.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1 and 5-9 are rejected under 35 U.S.C. 102(ab) as being anticipated by Chang et al. USP 5841165.

Figures 1, 2, and 3A of Chang are directed to a single-poly EEPROM, comprising: a first PMOS transistor (16) serially connected to a second PMOS transistor (18), wherein the first and second PMOS transistors are both formed on an N-well (12) of a P-type substrate (14), and

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therein the first PMOS transistor includes a floating gate (26), a first P+ doped drain region (20), and a first P + doped source region (22), the second PMOS transistor includes a gate (28) and second P + doped source region (24), and the first P + doped source region of the first PMOS transistor serves as a drain of the second PMOS transistor; and an erase gate (36 of fig. 1 or 2) formed in the P-type substrate in the vicinity of the first PMOS transistor (fig. 1), wherein the floating gate of the first PMOS transistor overlaps with the N-well and the P-type substrate and extends to the erase gate.

5. The prior art made of record and not relied upon is considered pertinent to applicants' disclosure. Kelly et al. (USP 622764 and 6191980), Fong et al. (USP 6215700) and Chern (USP 6166954) disclose a single-poly nonvolatile memory device.

Allowable Subject matter


6. Claims 2-4 and 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.


7. The following is a statement of reasons for the indication of allowable subject matter:

Claims include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure, taken individually or in combination, does not teach or suggest the claimed invention having wherein the erase gate is an N-type doped region formed in the P-type substrate beneath the floating gate in claim 2; and wherein pre-selected erase gate bias is positive, and the first doped drain region voltage is negative in claim 10.

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8. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.
9. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02 (b)).
10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to whose telephone number is (703) 308-4839. Other inquiries of this application should be called to (703) 308-0956 or the fax number (703) 308-7722.


H. Ho
June 26, 2003


Hoai V. Ho
Primary Examiner
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